REMARKS

Applicant concurrently files herewith a Petition and fee for a One-Month Extension of Time and an Excess Claim Fee Payment Letter and fee for excess independent claims.

Claims 1-7 and 13-16 are all the claims presently pending in the application. Claims 17-23 have been canceled. Claims 13-14 are allowed. Applicant gratefully acknowledges the Examiner's indication that claims 4-5 would be allowable if rewritten in independent form. These claims have been rewritten to place them into condition for immediate allowance.

It is noted that the claims have been amended solely to more particularly point out Applicant's invention for the Examiner, and not for distinguishing over the prior art, narrowing the claim in view of the prior art, or for statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached pages are captioned "**Version with markings to show changes made**".

Claims 1, 7, and 16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamazaki et al. (U.S. Patent No. 5,818,070)(hereinafter "Yamazaki").

Claims 2-3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Sakurai et al. (JP 10-290012)(hereinafter "Sakurai").

Claims 6 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Miyajima (JP 6-230425)(hereinafter "Miyajima").

These rejections are respectfully traversed in the discussion below.

I. THE CLAIMED INVENTION

Applicant's invention, as defined for example in independent claim 1, is directed to a thin film transistor having a back channel electrode (e.g., used in an active matrix type liquid crystal display panel in a non-limiting embodiment).

A feature of the invention is that a voltage of a front channel positioned on the side of a gate wiring of the thin film transistor may be made equal to a voltage of the back channel positioned on the side of a back channel electrode by short-circuiting the back channel electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming the thin film transistor.

An additional feature of the invention is that the semiconductor layer is patterned to have a width equal to that of source and drain electrodes of a thin film transistor between the source and drain electrodes and a gate insulating film.

With such features, a thin film transistor can be provided which is capable of reducing leakage current of a back channel when it is operated continuously (e.g. see page 3, lines 12-15; page 10, lines 7-27; page 11, lines 1-5; page 12, lines 17-27; and page 13, lines 1-7).

An exemplary configuration of the thin film transistor with a back channel electrode is shown in Figs. 2-3 of the application.

The conventional systems, such as those discussed below and in the Related Art section of the present application, do not have such a structure, and fail to provide for such an operation.

Indeed, such features are clearly not taught or suggested by the cited references.

II. THE PRIOR ART REFERENCES

A. The Yamazaki Reference

The Examiner asserts:

> *[regarding claim 1 and 16] Yamazaki disclose (see fig. 2, col. 2, lines 46-57 and col. 7, lines 6-11) a thin film transistor including a back channel electrode 114/115, wherein a voltage of a front channel positioned on a side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode 104-105 through a contact-hole (not shown) provided in a portion of a semiconductor layer having an ohmic contact layer on the side thereof, which is in contact with source and drain*

electrodes (as in claim 7) forming said thin film transistor.

[regarding claim 15] Yamazaki disclose (see fig. 2, col. 2, lines 46-57 and col. 7, lines 6-11) a thin film transistor including a back channel electrode 114/115, wherein a voltage of a front channel positioned on a side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode 104-105 through a contact-hole (not shown) provided in a portion of a semiconductor layer forming said thin film transistor, but fail to disclose a semiconductor layer having equal width as a source and drain electrodes.

Miyajima discloses in figs. 1-8 a semiconductor layer 15 patterned to have a width equal to a source and drain electrodes 25, 23 of a TFT provided between said source and drain electrodes and gate insulating film 14.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate Miyajima's teachings with the device of Yamazaki, since that would prevent shorting and improve yield as taught by Miyajima.

However, Applicant respectfully disagrees and submits that the Examiner's assertions are erroneous.

Firstly, regarding the rejection of independent claim 1 (e.g., and substantially similarly that of claims 7 and 16), Yamazaki discloses in Fig. 4B that the contact hole is provided in a portion of an insulating layer including silicon nitride films 110 and 106 (e.g., reference numeral 104 should read "106"). Yamazaki does not disclose or suggest providing the contact-hole in a portion of the semiconductor layer forming a thin film transistor. Thus, Applicant respectfully submits the Examiner's assertions that Yamazaki anticipates the present invention are erroneous.

Specifically, Yamazaki discloses "*the silicon nitride films 110 and 106 are etched to form contact holes which extend to reach the first gate lines*" (e.g., see column 7, lines 6-8 of Yamazaki). Thus, Yamazaki does not teach or suggest "*a voltage of a front channel positioned on the side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting*

said back channel electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming said thin film transistor", as defined by independent claim 1 (e.g., and substantially similarly by independent claim 16). As such, Yamazaki is unable to provide the advantages of the present invention including a thin film transistor which can be provided which is capable of reducing leakage current of a back channel when it is operated continuously.

Thus, turning to the clear language of independent claim 1 (and substantially similarly of independent claim 16), Yamazaki neither teaches nor suggests "*[a] thin film transistor including:*

a back channel electrode,

wherein a voltage of a front channel positioned on the side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming said thin film transistor " (emphasis Applicant's).

Thus, for the reasons stated above, claims 1, 7, and 16 of the present invention are fully patentable over the cited references.

Also, regarding claims 2-3 rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Sakurai, even assuming (arguendo) that Sakurai would have been combined with Yamazaki, the claimed invention still would not have been produced.

That is, Sakurai, as shown in Fig. 5, discloses providing a contact hole 7 in the insulating layer 103. There is no teaching or suggestion in Sakurai of a contact hole being provided in a portion of a semiconductor layer forming a thin film transistor. Specifically, there is no teaching or suggestion of "*short-circuiting said back channel electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming said thin film transistor* ", as defined by independent claim 1. Thus, claims 2-3, especially when taken in combination with claim 1, define additional novel limitations.

Similarly, regarding claims 6 and 15 rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki in view of Miyajima, even assuming (arguendo) that Miyajima would have been combined with Yamazaki, the claimed invention still would not have been produced.

For example, as shown in Fig. 8 of Miyajima, the semiconductor layer 15 is not patterned to have a width equal to that of source and drain electrodes 25 and 23 of a TFT between the source and drain electrodes 25 and 23 and a gate insulating film 14. Further, there is nothing in the disclosure of Miyajima which teaches, suggest or even alludes to such a feature of the claimed invention defined by claims 6 and 15.

Thus, even if they would have been combined (arguendo), Miyajima and Yamazaki do not teach or suggest "*said layer patterned to have a width equal to that of source and drain electrodes of said thin film transistor is provided between said source and drain electrodes and a gate insulating film of said film transistor*", as defined by independent claim 15 (and substantially similarly by dependent claim 6).

Further, the combination (arguendo) of Miyajima and Yamazaki would not teach or suggest "*short-circuiting said back channel electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming said thin film transistor*", as defined by independent claim 15.

Thus, all of claims 1-7 and 13-16 are patentable.

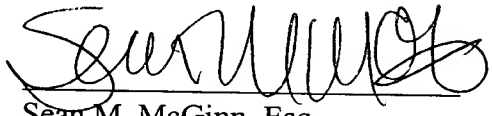
III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-7 and 13-16, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 17-23 have been canceled without prejudice or disclaimer.

The claims have been amended as follows:

4. (Amended) A thin film transistor [as claimed in claim 1,] including:

a back channel electrode,

wherein a voltage of a front channel positioned on the side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming said thin film transistor, and

wherein said contact-hole is formed in a location remote from an active region of said thin film transistor by at least five microns.

5. (Amended) A thin film transistor [as claimed in claim 1,] including:

a back channel electrode,

wherein a voltage of a front channel positioned on the side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming said thin film transistor, and

wherein a passivation film patterned to have a width equal to that of said back channel electrode and said semiconductor layer are provided between said back channel and a gate insulating film.

15. (Amended) A thin film transistor including:

a back channel electrode,

wherein a voltage of a front channel positioned on the side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming said thin film transistor, and

wherein said layer patterned to have a width equal to that of source and drain electrodes of said thin film transistor is provided between said source and drain electrodes and a gate insulating film of said film transistor.

16. (Amended) A thin film transistor including:

a back channel electrode,

wherein a voltage of a front channel positioned on the side of a gate wiring of said thin film transistor is made equal to a voltage of said back channel positioned on the side of a back channel electrode by short-circuiting said back channel electrode to a gate electrode through a contact-hole provided in a portion of a semiconductor layer forming said thin film transistor, and

wherein said layer has an ohmic contact layer on the side thereof, which is in contact with source and drain electrodes of said film transistor.